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10/801,103	03/15/2004	Neil S. Feiereisel	5150-85601	9259

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EXAMINER	
COSIMANO, EDWARD R	
ART UNIT	**PAPER NUMBER**
2863	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/801,103	FEIEREISEL ET AL.	
	Examiner	Art Unit	
	Edward R. Cosimano	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-95* is/are pending in the application.

4a) Of the above claim(s) *none* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-95* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20050218*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. The Oath/Declaration filed on 12 July 2004 and the Abstract filed on 15 March 2004 are acceptable to the examiner.

2. Applicant's claim for the benefit of an earlier filing date pursuant to 35 U.S.C. 119(e) is acknowledged.

3. Figures 2A, 2B, 4, 5, 6, 7 & 8, of the set of drawings containing 9 sheets of 10 figures are acceptable to the examiner where the set of drawings consists of figures 2A, 2B, 4, 5, 6, 7 & 8 as presented in the set of drawings filed on 15 March 2004.

4. The drawings filed on 15 March 2004 are objected to because:

A) the description of figure 1A in paragraph number 38 dose not describe what is depicted in figure 1A because as can be seen in figure 1A, one of ordinary skill at the time the invention was made would recognize the symbol used to represent "first signal 11" as a representation of a digital signal and the symbol used to represent "second signal 12" as a representation of an analog signal. In view of this applicant's references to "... the first signal 11 is an analog signal and the second signal 12 is a digital marker signal. In this embodiment, waveform generator 10 may send the analog signal (e.g., the second signal 12) to stimulate a UUT 17, and may trigger another device, such as a high-speed digitizer, with the digital marker signal (e.g., the first signal 11).", in paragraph number 38 is confusing. Note corresponding objection to the disclosure and the use of "first signal 11" and the "second signal 12" in paragraph number 37.

B) the drawings fail to comply with 37 CFR 1.84(p)(5) because they include the following reference legends not mentioned in the description, note reference legend 19 of figure 1A which has not been mentioned in the written description of figure 1A located in paragraph number 38, and note the corresponding objection to the disclosure.

C) the drawings fail to comply with 37 CFR 1.84(p)(5) because they do not include the following reference legends mentioned in the description, note reference legends 103b, 103c, 103d, 103e, 111, 112, 113, 114, 129b, 129c, 129d, 129e, 140b 140c, 140d, 140e, 145b, 145c, 145d, 145e, 150b, 150c, 150d, 150e & 180 of figure 3 which have been mentioned in the written description of figure 3 located in paragraph numbers 49, 76 & 98, and note the corresponding objection to the disclosure.

4.1 Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

5. The disclosure is objected to because of the following informalities:

A) applicant must update the application data with the current status of each reference application in on page 1 note now expired provisional application number 60/548,290. Note the suggested change to this paragraph below.

B) the following errors and/or inconsistencies between the drawings filed on 15 March 2004 and the written description have been noted:

(1) the description of figure 1A in paragraph number 38 dose not describe what is depicted in figure 1A because as can be seen in figure 1A, one of ordinary skill at the time the invention was made would recognize the symbol used to represent "first signal 11" as a representation of a digital signal and the symbol used to represent "second signal 12" as a representation of an analog signal. In view of this applicant's references to "... the first signal 11 is an analog signal and the second signal 12 is a digital marker signal. In this embodiment, waveform generator 10 may send the analog signal (e.g., the second signal 12) to stimulate a UUT 17, and may trigger another device, such as a high-speed digitizer, with the digital marker signal (e.g., the first signal 11).", in paragraph number 38 is

confusing. Note corresponding objection to the disclosure and the use of "first signal 11" and the "second signal 12" in paragraph number 37.

(2) if applicant chooses not to delete reference legend 19 from figure 1A, note above, then the written description fails to comply with 37 CFR 1.84(p)(5) because the written description does not include an explicit reference to this reference legend in the description of figure 1A located in paragraph number 38, and note the proposed changes below.

(3) the written description of figures 1A and 1B fails to comply with 37 CFR 1.84(p)(4) because the written description inconsistently references the "first signal" by using reference legends 11 & 12 and the "second signal" by using reference legends 11, 12 & 32 in paragraphs numbers 37-40 & 85-94 while describing figures 1A & 1B. In view of this it is suggested that applicant amend paragraph numbers 38-40 & 85-94 as indicated below.

(4) if applicant chooses not to add reference legends 103b, 103c, 103d, 103e, 111, 112, 113, 114, 129b, 129c, 129d, 129e, 140b 140c, 140d, 140e, 145b, 145c, 145d, 145e, 150b, 150c, 150d, 150e & 180 to figure 3, note above, then the written description fails to comply with 37 CFR 1.84(p)(5) because the written description includes an explicit reference to these reference legends in the description of figure 3 located in paragraph numbers 49, 76 & 98.

C) in view of the above objections it is suggested that the following paragraphs be amended as indicated:

(1) at page 1, lines 2-4:

This application claims benefit of priority of now expired U.S. provisional application Serial No. 60/548,290 titled "Automatic Delays for the Alignment of Data and Digital Markers", filed February 27, 2004, and whose inventors are Neil S. Feiereisel and Craig M. Conway.

(2) at paragraph number 38:

[0038] In the embodiment illustrated in FIG. 1A, waveform generator 10 is an arbitrary waveform generator, and the ~~first signal 11~~ second signal 12 is an analog signal

and the ~~second signal 12~~ first signal 11 is a digital marker signal. In this embodiment, waveform generator 10 may send the analog signal (e.g., the second signal 12) to stimulate a UUT 17, and may trigger another device, such as a high-speed digitizer 19, with the digital marker signal (e.g., the first signal 11).

(3) at paragraph number 39:

[0039] FIG. 1B illustrates a block diagram of one embodiment of a system comprising waveform generator 10 and a waveform generator 30 for generating a plurality of signals. It is noted that, as described above, each of waveform generators 10 and 30 may be any type of waveform generator. In one embodiment, the system may be operable to align signals from multiple sources. For example, in one embodiment, the system may be operable to align the output of a ~~first~~ second signal 12 (e.g., an analog signal) provided by a first source (e.g. waveform generator 10) and the output of a ~~second~~ third signal 32 (e.g., an analog signal) provided by a second source (e.g., waveform generator 30).

(4) at paragraph number 40:

[0040] In the embodiment illustrated in FIG. 1B, waveform generators 10 and 30 may be coupled together and may both be further coupled to a UUT 35. In one embodiment, some tests may require the UUT 35 to be stimulated by multiple signals simultaneously, even though the signals may have different signal characteristics. Therefore, in one embodiment, the system may comprise a delay determining unit which may be operable to determine a relative delay between the ~~first~~ second signal 12 provided by waveform generator 10 and the ~~second~~ third signal 32 provided by waveform generator 30, based upon a travel path of the ~~first~~ second signal 12 and a travel path of the ~~second~~ third signal 32. Furthermore, in one embodiment, the delay determining unit may be operable to program a delay circuit, based on a determined relative delay, to align the output of the ~~first~~ second signal 12 with the output of the ~~second~~ third signal 32 to test UUT 35.

(5) at paragraph numbers 85-94:

[0085] Referring back to FIG. 1B, the ~~first~~ second signal 12 provided by waveform generator 10 may be aligned in time with respect to the ~~second~~ third signal 32 provided by waveform generator 30 to test a particular device (e.g., a UUT 35). In one embodiment, each of waveform generators 10 and 30 may be a standalone waveform generator or a computer- based waveform generator. In one embodiment, each of waveform generators 10 and 30 may be an arbitrary waveform generators or a digital waveform generator (i.e., logic signal source). Furthermore, in one embodiment, each of waveform generators 10 and 30 may comprise one embodiment of circuit 101 as illustrated in the embodiments of FIG. 3 and FIG. 6 and may comprise the functionality of circuit 101 as described in the above embodiments with reference to FIG. 3-7.

[0086] In one embodiment, waveform generator 10 may be coupled to waveform generator 30. Waveform generators 10 and 30, in one embodiment, may be configured to receive user inputs specifying generation of signals. It is noted however that in other embodiments the signals may be created by other means, for example, by reproduction or modification of existing signals. In one embodiment, a delay determining unit, comprised in the system of FIG. 1B, may be operable to determine a relative delay between the ~~first~~ second signal 12 (e.g., an analog signal) provided by the waveform generator 10 and the ~~second~~ third signal 32 (e.g., an analog signal) provided by the waveform generator 30, based upon a travel path of the ~~first~~ second signal 12 and a travel path of the ~~second~~ third signal 32. Additionally, in one embodiment, the delay determining unit may be operable to program a data pipeline delay circuit, comprised in one of the waveform generators 10 and 30, based on the determined relative delay, to delay the output of one of the first and second signals to align the output of the ~~first~~ second signal 12 with the output of the ~~second~~ third signal 32.

[0087] FIG. 8 is a flow diagram illustrating a method for aligning the ~~first~~ second signal 12 provided by waveform generator 10 and the ~~second~~ third signal 32 provided by waveform generator 30. It should be noted that in various embodiments, some of the steps shown may be performed concurrently, in a different order than shown, or omitted. Additional steps may also be performed as desired.

[0088] Referring collectively to FIG. 1B, FIG. 3, and FIG. 8, as indicated in 710, in one embodiment, a delay determining unit may automatically determine a total path delay associated with a travel path of the ~~first~~ second signal 12 (e.g., an analog signal) and a total path delay associated with a travel path of the ~~second~~ third signal 32 (e.g., an analog signal).

[0089] In one embodiment, as indicated in 720, the delay determining unit may also automatically determine a relative delay between the ~~first~~ second signal 12 and the ~~second~~ third signal 32 by calculating the difference between the determined total path delay associated with the ~~first~~ second signal 12 and the determined total path delay associated with the ~~second~~ third signal 32.

[0090] In 730, the delay determining unit may also automatically program a data pipeline delay circuit, such as data pipeline delay circuit 120 comprised in waveform generator 100 (as shown in FIG. 3), based on the determined relative delay, to delay the output of one of the signals 12 and 32 to align the output of the ~~first~~ second signal 12 with the output of the ~~second~~ third signal 32, according to one embodiment. As described below in more detail, in some embodiments, further delay criteria may be considered in the determination of the delay to be programmed, including, for example, user specified offsets.

[0091] Lastly, in one embodiment, waveform generator 10 and waveform generator 30 may output the signals 12 and 32, respectively, as indicated in 740, where the output of the ~~first~~ second signal 12 is preferably aligned in time or sample number with respect to the output of the ~~second~~ third signal 32, in accordance with the determined relative delay. In one embodiment, the output of the ~~first~~ second signal 12 is from a first data path I/O terminal comprised in waveform generator 10 and the output of the ~~second~~ third signal 32 is from a second data path I/O terminal comprised in waveform generator 30. It is noted however that in other embodiments the delay determining unit may be operable to program a first data pipeline delay circuit comprised in waveform generator 10 and a second data pipeline delay circuit comprised in waveform generator

30 to align the output of the ~~first~~ second signal 12 with the output of the ~~second~~ third signal 32.

[0092] In one embodiment, delay determining unit may be operable to receive a user input indicating an additional delay to program the data pipeline delay circuit to add the determined relative delay plus the additional delay to the output of the ~~first~~ second signal 12 to output the ~~first~~ second signal 12 at a predetermined position with respect to the output of the ~~second~~ third signal 32. For example, the user input may indicate to add an additional delay of 6 samples to the output of the ~~first~~ second signal 12. It is noted that in other embodiments a user may specify the additional delay in the waveform generators by entering a delay value in terms of time or number of samples.

[0093] In one embodiment, delay determining unit may be operable to receive a user input reducing the determined relative delay to program the data pipeline delay circuit to add the reduced relative delay to the output of the ~~first~~ second signal 12 to output the ~~first~~ second signal 12 at a predetermined position with respect to the output of the ~~second~~ third signal 32. For example, the user input may indicate to reduce the determined delay by 2 samples.

[0094] In one embodiment, a user of waveform generator 10 may temporarily disable the automatic delay determining capabilities of delay determining unit. Instead, in this embodiment, the user may program the corresponding data pipeline delay circuit with a desired delay value to delay output of the ~~first~~ second signal 12 to output the ~~first~~ second signal 12 at a predetermined position with respect to the output of the ~~second~~ third signal 32. In one embodiment, delay determining unit may be operable to receive a user input to program the corresponding data pipeline delay circuit with the desired delay value.

5.1 Appropriate correction is required.

6. Claims 18-25 are objected to because of the following informalities.

6.1 Claim 18-25 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Note the rejection of these

claims below in section 7.1.3. Applicant is required to cancel the claims, or amend the claims to place the claims in proper dependent form.

6.2 Appropriate correction is required.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7.1 Claims 1-95 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7.1.1 In regard to claims 1-95, as the invention recited in these claims would be reasonably interpreted by one of ordinary skill at the time the invention was made, these claims recite an invention that determines a the propagation delay for a first signal and a second signal in order to determine the relative delay between the first signal and the second signal. Next the claimed invention uses the determined relative delay in order to program a programmable machine/process in order to delay a first one of the two signals to occur at a particular relative time or relative position with respect to the second one of the two signals.

7.1.1.1 It is further noted that one of ordinary skill at the time the invention was made would reasonably interpret the claimed invention as not positively reciting a requirement that the function or action of delaying the first one of the two signals in any manner so that the delayed first signal would in fact occur at a particular relative time or relative position with respect to the second one of the two signals.

7.1.1.2 Since the claimed invention merely makes a vague, indefinite and unclear allusion to programming a machine/process to perform a function or action that is not positively recited as being performed by the claimed invention, then one of ordinary skill at the time the invention was made would be confused by how the claimed invention could which lacks the essential subject that would permit the claimed invention to provide the credible, substantial, useful and beneficial function of delaying a first one of the two signals to occur at a particular relative time or relative position with respect to the second one of the two signals.

7.1.1.3 In regard to the above, note that one of ordinary skill would not be able to ascertain either: (1) what applicant intends as being included as part of the claimed invention; or (2) what the inventor's contribution to the prior art is and hence the scope of the claim, In re Larsen, No. 01-1092 (Fed. Cir. May 9, 2001) (unpublished) "The court observed that the totality of all the limitations of the claim and their interaction with each other must be considered to ascertain the inventor's contribution to the art. Upon review of the claim in its entirety, the court concluded that the claim at issue apprises one of ordinary skill in the art of its scope and, therefore, serves the notice function required by 35 U.S.C. 112 paragraph 2.".

7.1.2 In regard to claims 18-25, because claim 1 recites a process and claims 16-25 recite a machine, then one of ordinary skill at the time the invention was made would be confused by the dependency of machine claims 16-25 either directly or indirectly from process claim 1.

7.1.3 Further since claims 18-25 appear to recite the same subject matter as recited in claims 2-9, respectively, then one of ordinary skill at the time the invention was made would be confused by the how the dependency of machine claims 16-25 either directly or indirectly from process claim 1 would clearly and distinctly point out an invention that is different from the invention recited in claims 2-9. In this regard it is noted that maybe claims 18-23 should depend from machine claim 17.

7.1.4 In regard to claims 26-28, since claim 17 fails to positively recite performing the function of "automatically determining the delay", then one of ordinary skill at the time the invention was made would be confused by the how the positively recited function of "automatically determining a delay" as positively recited in claims 26-28 would find antecedent basis in claim 17. In this regard it is noted that maybe claim 26 should be dependent from for example claim 23.

7.1.5 For the above reasons applicant has failed to particularly and distinctly point out what is regarded as the invention. Claims not explicitly mentioned above, inherent each the described problems through dependency to the explicitly mentioned base claim.

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8.1 Claims 1-95 are rejected under 35 U.S.C. 103(a) as being unpatentable over either Cebula (3,866,126) or Suzuki (5,253,243) or Orihashi et al (5,406,198 or 5,438,259) or Alger-Meunier et al (6,252,890) or Higashide (2002/0013672 or 6,556,934 or 2003/0125897) as these reference would be reasonably interpreted by one of ordinary skill at the time the invention was made.

8.1.1 In regard to claims 1-95, either Cebula ('126) or Suzuki ('243) or Orihashi et al ('198 or '259) or Alger-Meunier et al ('890) or Higashide ('672 or '934 or '897) disclose a machine/process that uses a measures delay in order to correct the operation of a machine/process. In this regard it is noted that:

A) Cebula ("126) provides the useful and beneficial function of determining the interval or delay between two events in which a machine/process is used to determine the interval to be measured by correcting the measured interval with correction amount that is based on the propagation delays of the measuring circuit and which is subtracted from the measured interval.

B) Suzuki ('243) provides the useful and beneficial function of starting the recording of a signal after a variable delay in which a variable delay line is used to generate the triggering pulses that are used in order to cause the machine/process to record the value of a signal.

E) either Orihashi et al ('198 or '259) provides the useful and beneficial function of correcting the operation of a machine/process for various delays in which a machine/process is used to determine the propagation delays of the components of the machine/process to be corrected and the determined propagation delay is used to correct the operation of the machine/process.

F) Alger-Meunier et al ('890) that provides the useful and beneficial function of synchronizing data/information by measuring the transit time differences or delays between various machines/process and then inserting various delays into the data/information at a machine/process in order to time synchronize event in the data/information.

G) either Higashide ('672 or '934 or '897) that provides the useful and beneficial function of correcting for differences in the interval or delay associated with different signal processing paths or circuits in which a machine/process is used to determine and store the interval or delay for each signal processing path/circuit and then when the associated signal processing path/circuit is to be used, the stored interval or delay is subtracted from the measured delay or interval in order to compensate or correcting the measured interval or delay for the propagation delays of the corresponding signal processing path/circuit.

Although each of these references disclose different circuits to perform the same function in different fashions, as one of ordinary skill at the time the invention was made would interpret the teachings of these references, it would have been obvious to one of ordinary skill at the time the invention was made that as can be seen that each of each of either Cebula ('126) or Suzuki ('243) or Orihashi et al ('198 or '259) or Alger-Meunier et al ('890) or Higashide ('672 or '934 or '897) these references teaches the function of determining a relative delay between two signals based on the signal processing paths/circuits being used by each of the signals. Once the relative delay has been determined, the determined relative delay is used by an appropriate type of programmable variable delay device in order to add a variable delay to the signal processing path of a first one of the signals in order to time align the corresponding first one of the signals to a particular position/location relative to the other one of the signals.

8.1.2 In regard to claims 4-6, 18-20, 58, 59, 62-65 & 73, since each of either Cebula ('126) or Suzuki ('243) or Orihashi et al ('198 or '259) or Alger-Meunier et al ('890) or Higashide ('672 or '934 or '897) disclose machines/process that functions to align two different signals, it would have been obvious to one of ordinary skill at the time the invention was made that any suitable type of signal could be aligned by the machines/process of each of either Cebula ('126) or

Suzuki ('243) or Orihashi et al ('198 or '259) or Alger-Meunier et al ('890) or Higashide ('672 or '934 or '897).

8.1.3 In regard to claims 7-16, 21-30, 32-41, 43-56, 60, 66-72, 75-85 & 87-95, since each of either Cebula ('126) or Suzuki ('243) or Orihashi et al ('198 or '259) or Alger-Meunier et al ('890) or Higashide ('672 or '934 or '897) disclose machines/process that functions to align two different signals based on the delay introduced by the signal processing paths, it would have been obvious to one of ordinary skill at the time the invention was made that any suitable representation, for example, a fixed delay or a variable delay for each of the elements of the signal processing paths would need to be considered in order to accurately determine the signal processing delays of the signal path and thereby accurately align the first signal to the second signal with in the machines/process of each of either Cebula ('126) or Suzuki ('243) or Orihashi et al ('198 or '259) or Alger-Meunier et al ('890) or Higashide ('672 or '934 or '897).

8.1.4 In regard to claim 57, since each of either Cebula ('126) or Suzuki ('243) or Orihashi et al ('198 or '259) or Alger-Meunier et al ('890) or Higashide ('672 or '934 or '897) disclose machines/process that functions to accurately align two different signals based on the delay introduced by the signal processing paths, and it is well known that the operating temperature of a machine/process may affect the operation of the machine/process, then it would have been obvious to one of ordinary skill at the time the invention was made that if the operating temperature would affect the operation of the machine/process of each of either Cebula ('126) or Suzuki ('243) or Orihashi et al ('198 or '259) or Alger-Meunier et al ('890) or Higashide ('672 or '934 or '897) then the machine/process of each of either Cebula ('126) or Suzuki ('243) or Orihashi et al ('198 or '259) or Alger-Meunier et al ('890) or Higashide ('672 or '934 or '897) must consider variations in the operating temperature in order to accurately align the first signal to the second signal.

9. The examiner has cited prior art of interest, for example:

A) either Grumet et al (2,768,348) or Myers (2,887,653) or Kronacher (2,896,160) or Isley, Jr. (2,994,822) or Takenaka et al (JP 61-14580 A) or Bolkow et al (4,569,599) or Ohishi et al (4,942,561) or Goldberg et al (5,201,061) or Ohtaki et al (5,633,709) disclose a machine/process that provides the useful and beneficial function of

determining the interval or delay between two events or signals or pulses in which a machine/process is used to determine the interval to be measured, see for example the use of an integrator in either Grumet et al (2,768,348) or Isley, Jr. (2,994,822) or the counting of clock pulses in either Myers (2,887,653) or Kronacher (2,896,160).

B) Chiang (3,070,305) disclose a machine/process that provides the useful and beneficial function of generating a predetermined amount of a delay by using a plurality of delay elements that may be selectively added or subtracted from a signal line in order to provide a determined amount of delay to the signal.

C) either Giral et al (2006/0074584 or 2006/0085157 or 7,099,792 or 7,177,777) or Yamazaki et al (2006/0150019) Negishi (2007/0011634) disclose a machine/process for solving the same problem as the instant invention but have an effective filing date after the 15 March 2004.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edward R. Cosimano whose telephone number is 571-272-0571. The examiner can normally be reached on 571-272-0571 from 7:30am to 4:00pm (Eastern time).

10.1 If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow, can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10.2 Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ERC
01/18/2008

Edward Cosimano

Edward Cosimano
Primary Examiner